PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G06F 7/00 // H04L 12/56

A1

(11) International Publication Number: WO 98/43159

(43) International Publication Date: 1 October 1998 (01.10.98)

(21) International Application Number: PCT/FI98/00257

(22) International Filing Date: 23 March 1998 (23.03.98)

(30) Priority Data:
971284 26 March 1997 (26.03.97) FI

(71) Applicant (*for all designated States except US*): OY NOKIA AB [FI/FI]; Etaläesplanadi 2, FIN-00130 Helsinki (FI).

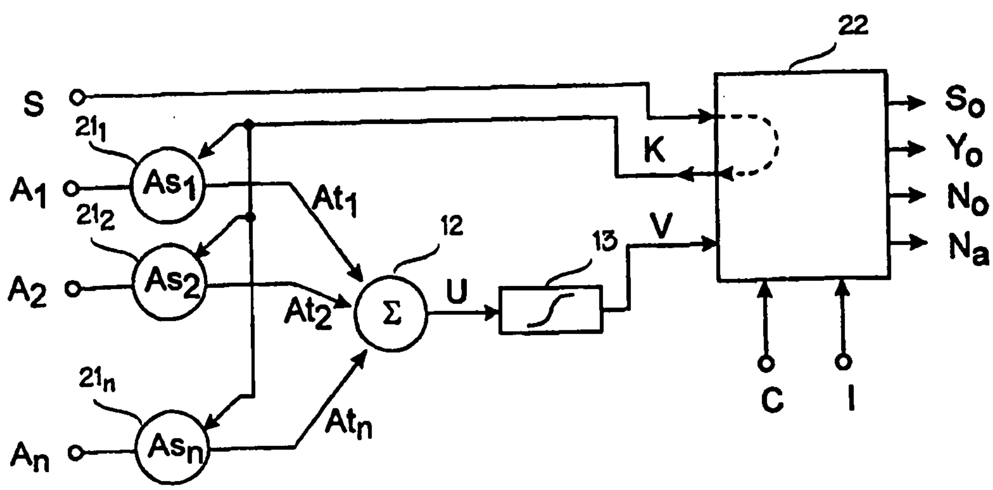
(72) Inventor; and
(75) Inventor/Applicant (*for US only*): HAIKONEN, Pentti [FI/FI]; Vernonrinne 17 E, FIN-00370 Helsinki (FI).

(74) Agent: KOLSTER OY AB; Iso Roobertinkatu 23, P.O. Box 148, FIN-00121 Helsinki (FI).

(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.
In English translation (filed in Finnish).

(54) Title: ASSOCIATIVE NEURON IN AN ARTIFICIAL NEURAL NETWORK



(57) Abstract

An associative artificial neuron comprises means for receiving a number of auxiliary input signals (A_1 to A_n); means for forming from them a sum (U) weighted by coefficients (W_1 to W) and means (13) for applying a non-linear function to the weighted sum (U) to generate a non-linear signal (V). In the invention the neuron further comprises means for receiving a main input signal (S) and means (22) for forming, on the basis of the main signal (S) and the non-linear signal, the function [(S_o) S] OR V, which is used to generate a main output signal, and at least one of the three logical functions Y_o=S AND V, N_o=NOT S AND V, N_a=S AND NOT V, and for using the thus obtained logical function to generate an additional output signal for the neuron.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece	ML	Mali	TR	Turkey
BG	Bulgaria	HU	Hungary	MN	Mongolia	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MR	Mauritania	UA	Ukraine
BR	Brazil	IL	Israel	MW	Malawi	UG	Uganda
BY	Belarus	IS	Iceland	MX	Mexico	US	United States of America
CA	Canada	IT	Italy	NE	Niger	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NL	Netherlands	VN	Viet Nam
CG	Congo	KE	Kenya	NO	Norway	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NZ	New Zealand	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	PL	Poland		
CM	Cameroon	KR	Republic of Korea	PT	Portugal		
CN	China	KZ	Kazakstan	RO	Romania		
CU	Cuba	LC	Saint Lucia	RU	Russian Federation		
CZ	Czech Republic	LI	Liechtenstein	SD	Sudan		
DE	Germany	LK	Sri Lanka	SE	Sweden		
DK	Denmark	LR	Liberia	SG	Singapore		
EE	Estonia						

ASSOCIATIVE NEURON IN AN ARTIFICIAL NEUTRAL NETWORK

BACKGROUND OF THE INVENTION

The invention relates to an associative neuron used in artificial neural networks.

In artificial neural networks, neurons derived from the McCullogh-Pitts (1943) neuron, such as different versions of the perceptron (Frank Rosenblatt 1957), are used. Neural networks are discussed, for example, in the article "Artificial Neural Networks: A Tutorial" by Anil K. Jain, Jianchang Mao and K.M. Mohiuddin in *IEEE Computer*, March 1996, p. 31 to 44.

In Fig. 1, signals X_1 to X_n are inputs of an artificial neuron and Y is its output signal. The values of the input signals X_1 to X_n can be continuously changing (analogous) or binary quantities, and the output signal Y can usually be given both positive and negative values. W_1 to W_n are weighting coefficients, i.e. synaptic weights, which can also be either positive or negative. In some cases, only positive signal values and/or weighting coefficients are used. Synapses 11_1 to 11_n of the neuron weight the corresponding input signal by the weighting coefficients W_1 to W_n. A summing circuit 12 calculates a weighted sum U. The sum U is supplied to a thresholding function circuit 13, whose output signal is V. The threshold function can vary, but usually a sigmoid or a piecewise linear function is used, whereby the output signal is given continuous values. In a conventional neuron, the output signal V of the thresholding function circuit 13 is simultaneously the output signal Y of the whole neuron.

When neurons of this kind are used in artificial neural networks, the network must be trained, i.e. appropriate values must be found for the weighting coefficients W_1 to W_n. Different algorithms have been developed for the purpose. A neural network that is capable of storing repeatedly supplied information by associating different signals, for example a certain input with a certain situation, is called an associative neural network. In associative neurons, different versions of what is known as the Hebb rule are often used. According to the Hebb rule, the weighting coefficient is increased always when the input corresponding to the weighting coefficient is active and the output of the neuron should be active. The changing of the w ighting co fficients according to the algorithms is called the training of th n ural network.

From previously known artificial neurons, it is possible to assemble neural networks by connecting neurons in parallel to form layers and by

arranging the layers one after the other. Feedback can be impl m nted in the networks by feeding output signals back as input signals. In wide networks assembled from neurons, however, the meaning of individual signals and even groups of signals is blurred, and the network becomes more difficult to design and manage. To produce an attention effect, for example, the network operations would have to be strengthened in one place and weakened in another, but the present solutions do not provide any clear answers to where, when and how this should be done, and in what way.

BRIEF DESCRIPTION OF INVENTION

The object of the invention is to provide a method and equipment implementing the method in which the above problems of training a neural network can be solved. To put it more precisely, the object of the invention is to provide a mechanism by which useful additional information can be produced on the level of an individual neuron about the relations between the different input signals of the neuron. The mechanism must be flexible and versatile to make artificial neurons widely applicable. The mechanism must also be fairly simple so that the costs of manufacturing neurons can be kept low.

The object of the invention is achieved by a method and equipment that are characterized by what is stated in the independent claims. The preferred embodiments of the invention are claimed in the dependent claims.

The invention is based on expansion of a conventional neuron such that a specific expansion, i.e. nucleus, is attached to the conventional neuron, a specific main input signal, i.e. main signal, passing through the nucleus. The nucleus keys and adjusts the main signal by a signal obtained from the conventional part of the neuron, and forms between these signals logical operations and/or functions needed to control neural networks. The processing power of a single neuron is thus increased as compared with the previously known neurons, which process data only by means of weighting coefficients and threshold functions. On the other hand, a clear distinction between main signals and auxiliary signals makes neural networks easier to design, since the training according to the Hebb rule is then easy to implement in such a way that each weighting coefficient is increased always when the main signal and the auxiliary input signal concerned are simultan ously active.

On the basis of the main signal (S) and a non-linear signal (V), the function (S_o)S OR V is formed in the neuron of the inv ntion and us d to

generate a main output signal, and in addition, at least one of the three logical functions Y_O=S AND V, N_O=NOT S AND V, N_a=S AND NOT V is formed and used to generate an additional output signal for the neuron.

The neuron of the invention and the network consisting of such neurons learn quickly: even one example may suffice. The operation of the neuron of the invention and that of the networks consisting of such neurons are simple and clear.

BRIEF DESCRIPTION OF DRAWINGS

The invention will now be described in greater detail by means of preferred embodiments and with reference to the attached drawings, in which

Fig. 1 is a general view of an artificial neuron,

Fig. 2 is a general view of a neuron of the invention,

Fig. 3 is a block diagram of the neuron of the invention, and

Figs. 4 to 6 illustrate ways of implementing specific details of the neuron of the invention.

DETAILED DESCRPTION OF INVENTION

In Fig. 2, the neuron according to a preferred embodiment of the invention comprises a main signal input S, an arbitrary number of auxiliary signal inputs A_1, A_2, ..., A_n, at least one controlling input C and at least one inhibiting input I, and a number of outputs. In the example of Fig. 2 the main output signal of the neuron is S_O, and Y_O, N_O and N_a (or one/some of them) are auxiliary output signals. The input and output signals can be, for example, voltage levels.

Blocks 21_1, 21_2, ..., 21_n are synapses of the neuron, in which the weighting coefficient corresponding to the auxiliary signal A_1, A_2, ..., A_n concerned is stored. In practice, the synapses are, for example, circuit units. Block 12 is a summing circuit, in which the output signals At_1, ..., At_3 of the synapses 21_1, 21_2, ..., 21_n are summed. Block 13 is a thresholding circuit, which can be implemented simply as a comparator, which supplies an active output signal only if its input signal level, i.e. the output signal level of the summing circuit 12, exceeds a pre-set threshold value.

Block 22 compris s the neuron expansions of the invention. In the present application, the expansions are call d the nucl us of the neuron. The function of the nucleus is, for xampl , to key and adjust th main signal S on the basis of the output signal of the thresholding circuit 13 and to form logical

operations and/or functions between the signals. Particularly us ful logical operations are the logical OR (signal S_O) and the logical AND (signal Y_O). Other logical operations can also be used in the same way as AND so that the main signal S is inverted first (signal N_O) or so that the output signal V of the thresholding circuit 13 is inverted first (signal N_a).

In a preferred embodiment of the invention, the nucleus 22 also comprises circuitry that deactivates the output signal S_O when a certain period of time has passed from the initiation of the signal, irrespective of what happens in the inputs of the neuron. The circuitry can also take care that a new output pulse cannot be initiated until a certain period of recovery has passed. To the nucleus 22 can also be connected an inhibiting input signal I (Inhibit), which inhibits all outputs when activated (forces them to an inactive state). The control input signal C (Control) controls the synapses' learning.

Fig. 3 is a block diagram of a neuron of the invention, the neuron here comprising three auxiliary signal inputs A_1 to A_n and therefore three synapses 21_1 to 21_3 in addition to the main signal input. The expanded neuron of the invention can be implemented in various ways within the scope of the inventive idea disclosed above.

Figs. 4 to 6 show an embodiment of the neuron according to the present invention in which the input and output signals are voltage signals. In the embodiment of Figs. 4 to 6 the signal is called 'active', if its voltage is positive, and 'inactive', if its voltage is substantially zero.

Fig. 4 shows a way of implementing the synapses 21_1 to 21_n of the neuron of Fig. 3. In this solution the voltage corresponding to the weighting coefficient of the synapse is stored through a resistor 41 and a diode 42 in a capacitor 43 always when auxiliary signal A_1 and the main signal S are simultaneously active. (A possible association between the main signal S and the key signal K is described in connection with gate 632 of Fig. 6.) The resistor 41 and the capacitor 43 define a time constant by which the voltage of the capacitor 43 grows. The diode 42 inhibits the voltage from discharging through an AND gate 40. The voltage of the capacitor 43 is supplied to an operational amplifier 44 functioning as a voltage follower, the input impedance of the amplifier being very high (i.e. the discharging of the capacitor 43 caused by it is negligible). Th output of the synapse is signal At_1, which is obtained from input signal A_1 by locking it at th voltag level corresponding to the weighting coefficient by a diode 45 and a resistor 46. A second voltage

follower 47 buffers the output signal. Always when input signal A_1 is active, output signal At_1 is proportional to the current value of the weighting coefficient.

Fig. 5 shows a way of implementing the summing block 12 of the neuron of Fig. 3. The voltages At_1 to At_3 obtained from synapses 21_1 to 21_3 are summed by a resistor network 50 to 53. (It is readily noticeable that the number of the inputs At_1 to At_3 and that of the resistors 51 to 53 are arbitrary.) The thresholding is performed by a comparator 54, and the thresholding is here abrupt so that the output of the comparator 54 is active only when the summed voltage U in the positive input of the comparator 54 exceeds the threshold value in the negative input (the threshold value in the example of Fig. 5 being the output voltage of a constant voltage power source 55).

Fig. 6 shows a way of implementing the nucleus 22 of the neuron of Fig. 3. An OR circuit 602 generates a main output signal S_O if the inputted main signal S is active or the thresholded summed voltage V is active. The nucleus 22 contains a block 606, indicated by a dotted line, functioning as a delay circuit. In the example of Fig. 6 the delay circuit 606 comprises a buffer 608 and an inverter 610, resistors 612 to 614 and capacitors 616 to 618. Normally the output of the delay circuit 606 is active, so an AND gate 604 allows an output signal to pass through. When the delay caused by the structure of the components of the delay circuit 606 has passed, the output pulse, inverted, reaches the AND gate 606 and deactivates the main output S_O. S_O cannot be re-activated until the delayed output pulse in the output of the delay circuit 606 has ended. A logical AND operation Y_O is formed by AND circuit 620: the first element in the operation is the main signal S and the second element is a summed signal V weighted by the weighting coefficients of the auxiliary signals A_1 to A_n and subsequently thresholded. A corresponding AND operation N_O is formed by AND circuit 622, with the exception that the inverse value of the main signal S has been first formed (i.e. the signal has been inverted) by NO circuit 626. The corresponding AND operation N_a is formed by AND circuit 624, with the exception that the thresholded summed signal V has been first inverted by NO circuit 628. All the outputs can be inhibited by an I signal, which is (here) inverted by NO circuit 630 and then supplied, in the inverted form, to AND circuits 620 to 624. The synapses are controlled by a K signal in accordanc with the Hebb rul (cf. Fig. 2). A control signal C is used to define when learning is allowed at all. The

generation of the key signal K is inhibited by AND circuit 632 when the control signal C is inactive.

The additional output signals Y_O, N_O and N_a of the neuron according to the invention can be used, for example, as follows. An active signal Y_O (Y = "Yes") means that the main signal S and the auxiliary signals A correspond to each other, i.e. they have been associated. An active signal N_O (N = "No) means that the main signal S and the auxiliary signals A do not correspond to each other. The auxiliary signal A is thus active, but the main signal S is not. An active signal N_a ("No association) indicates a situation where the main signal S is active but the auxiliary signal A is not. One characteristic of the neural network is its ability to predict a situation. An active signal N_a indicates that there is a new input signal S which is not predicted by the auxiliary signals A. Signal N_a is thus a 'surprise indicator', which can be used to draw attention to new, surprising signals.

The control signal C controls, or keys, the K signal. It is not expedient for the network to learn all the situations that occur. When a normal human being encounters a new situation, he/she either concludes or instinctively knows whether the situation is worth learning. This kind of focusing of attention can be simulated by the control signal C.

In the above example the auxiliary signals A_1 to A_n can be given continuously changing values and the main signal S can be given two different values. The threshold function is here a simple comparative operation. The invention is not limited to the above, but it can be applied more broadly, for example, so that the main signal S and the key signal K can also be given continuous values. The threshold function can be replaced with any appropriate non-linear continuous or step function. The neuron's learning is then not limited to two mutually exclusive situations: allowed or inhibited. Instead, the learning process is divided into different degrees or it is a continuum of degrees, whereby the strength of the K signal is adjusted on the basis of the main signal S. In the normal state of the neural network (when the network is not being trained), the key signal K is not more than a fraction of the main signal S, if the S signal is active. When the network is to be trained, the value of the key signal K approaches the value of the main signal S. In practice, the binary AND gates in Figs. 4 and 6 should be replaced, for example, with analogue multipliers or adjustable amplifiers or attenuators or the like.

In practice, a huge number of neurons (usually 10^4 to 10^6) are needed in neural networks. The neuron of the invention can be implemented by a process suitable to large-scale integration, for example by the EEPROM technique, which is used to manufacture the speech storage circuits implemented by semi-conductors. Alternatively, the neurons and the neural network can be simulated by a computer program executed in a digital processor. The values corresponding to the weighting coefficients of the synapses of the neurons are here stored in memory locations (e.g. in a matrix variable) and the other parts of the neuron are implemented by software logic.

The invention can be applied in areas where information is processed using extensive artificial neural networks. The areas include, for example, processing of audiovisual information, interpretation of sensory information in general and of speech and image in particular, and formation of response. The invention is applicable in many modern fields of industry, such as human/machine interfaces, personal electronic assistants and/or means of communication, multimedia, virtual reality, robotics, artificial intelligence and artificial creativity.

It will be obvious to a person skilled in the art that with the advancement of technology, the basic idea of the invention can be implemented in many different ways. The invention and its embodiments are thus not limited to the above examples but they can vary within the scope of the claims.

CLAIMS

1. A method of forming output signals of an associative artificial neural network by

receiving a number of auxiliary signals (A_1 to A_n);

forming a corresponding weighting coefficient (W_1 to W_n) for each auxiliary signal (A_1 to A_n);

forming from the auxiliary signals (A_1 to A_n) a sum (U) weighted by the corresponding coefficients (W_1 to W_n);

applying a non-linear function to the weighted sum (U) to generate a non-linear signal (V);

characterized by

receiving a main signal (S), which can be associated with the auxiliary signals (A_1 to A_n) such that the weighting coefficient (W_1 to W_n) of each auxiliary signal is increased when the main signal (S) and the corresponding auxiliary signal (A_1 to A_n) are simultaneously active;

forming, on the basis of the main signal (S) and the non-linear signal (V), a function (S_O) S OR V, which is used to generate a main output signal, and at least one of the three logical functions Y_O=S AND V, N_O=NOT S AND V, N_a=S AND NOT V, and using said logical function to generate an additional output signal for the neuron.

2. An associative artificial neuron comprising

means (11_1 to 11_n; 21_1 to 21_n) for receiving a number of auxiliary signals (A_1 to A_n) and forming a corresponding coefficient (W_1 to W_n) for each auxiliary signal (A_1 to A_n);

means (12) for forming from the auxiliary signals (A_1 to A_n) a sum (U) weighted by the corresponding coefficients (W_1 to W_n);

means (13) for applying a non-linear function to the weighted sum (U) to generate a non-linear signal (V);

characterized by further comprising

means for receiving a main signal (S)), which can be associated with the auxiliary signals (A_1 to A_n) such that the weighting coefficient (W_1 to W_n) of each auxiliary signal is increased when the main signal (S) and the corresponding auxiliary signal (A_1 to A_n) are simultaneously active; and

means (22) for forming, on the basis of th main signal (S) and the non-linear signal (V), a function (S_O) S OR V, which is us d to generate a main output signal, and at least one of the three logical functions Y_O=S AND V,

N_O=NOT S AND V, N_a=S AND NOT V, and using the thus obtained logical function to generate an additional output signal for the neuron.

3. A neuron according to claim 2, **characterized** by said non-linear function being a threshold function and the non-linear signal (V) obtained by the function having a first state and a second state.

4. A neuron according to claim 2, **characterized** by the non-linear function being a step function with more than two steps.

5. A neuron according to claim 2, **characterized** by the non-linear function being a continuous function.

6. A neuron according to claim 2, **characterized** by the main output signal (S_O) having a first state and a second state and the neuron further comprising means (606) for setting an upper limit to the length of time that said main output signal (S_O) is in the second state.

7. A neuron according to claim 6, **characterized** by the neuron further comprising means (606) for setting a lower limit to the length of time that said main output signal (S_O) remains in the first state after having been in the second state.

8. A neuron according to any one of claims 2 to 7, **characterized** by further comprising means (40, 632) for adjusting the neuron's learning in response to an external control signal (C).

9. A neuron according to claim 8, **characterized** by the means (40, 632) for adjusting the neuron's learning having two states, whereby the neuron's learning is either allowed or inhibited.

10. A neuron according to any one of claims 2 to 9, **characterized** by further comprising means (630, 604, 620 to 624) for forcing at least one ouput signal (S_O, Y_O, N_O, N_a) to a predetermined state in response to an external inhibiting signal (I).

Fig. 1

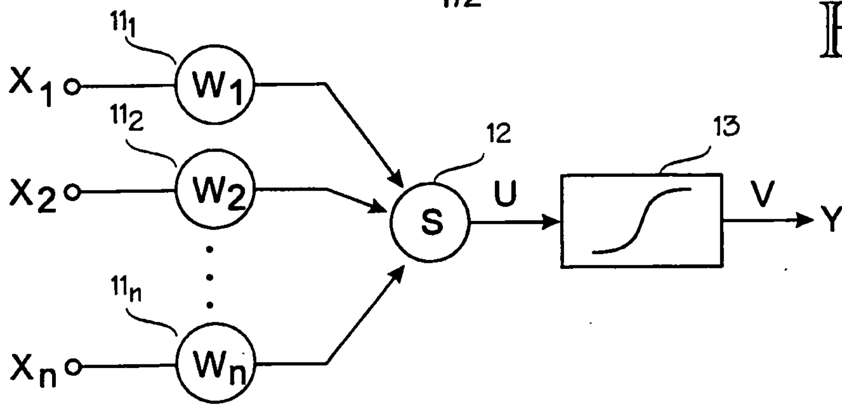


Fig. 2

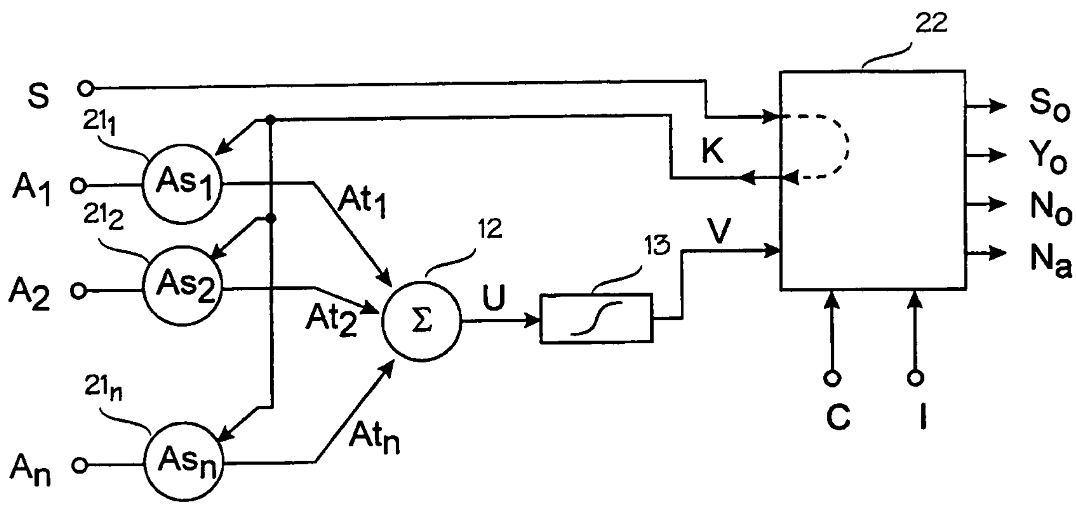


Fig. 3

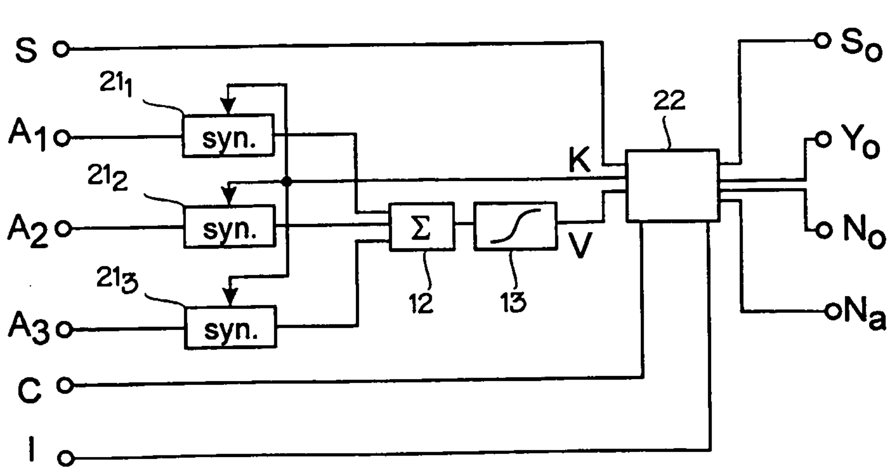


Fig. 4

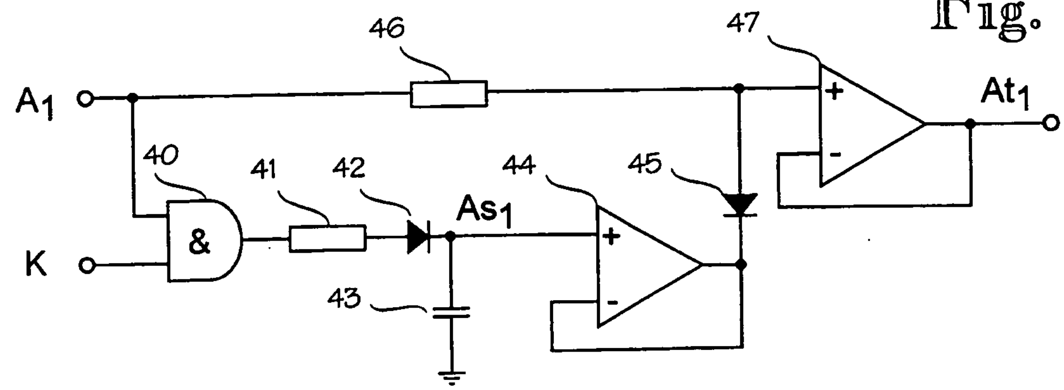


Fig. 5

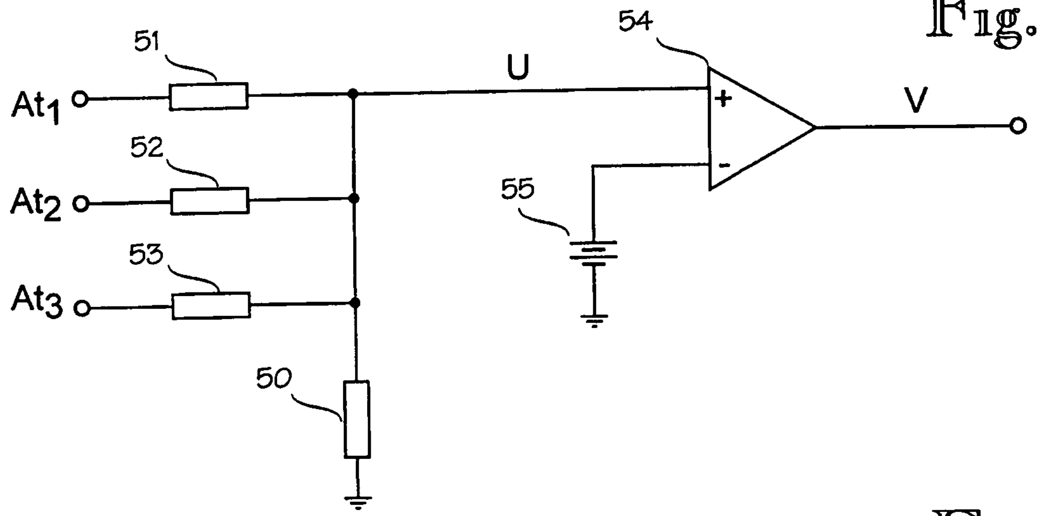
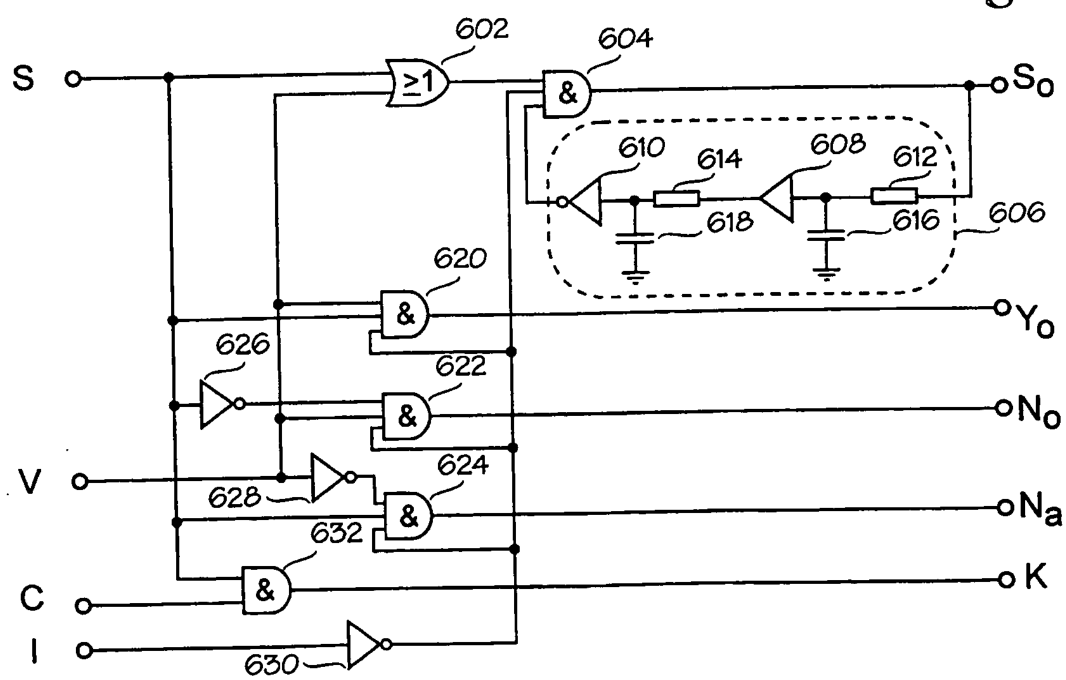


Fig. 6



INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI 98/00257

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: G06F 7/00 // H04L 12/56

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: G06F, H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5535309 A (Y-C,SHIN ET AL), 9 July 1996 (09.07.96), column 2, line 25 - line 38; column 6, line 31 - line 40; column 8, line 12 - line 32, figures 1,2,3, abstract --	1-5,8-10
A	US 5467429 A (K.UCHIMURA ET AL), 14 November 1995 (14.11.95), column 8, line 17 - column 9, line 10, figures 30,31, abstract --	1-5,8-10
A	US 5299285 A (R.TAWEL), 29 March 1994 (29.03.94), see the whole document --	1,2

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" erlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 August 1998	07 -08- 1998

Name and mailing address of the ISA/	Authorized officer
Swedish Patent Offic Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Bj¨rn Edlund Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI 98/00257

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	IEEE COMPUTER, Volume 29, No 3, March 1996, ANIL K. JAIN et al., "Artificial Neural Networks: A Tutorial", page 31 - page 44, page 34: ANN Overview computational models of neurons, Network architectures.	1,2

--

INTERNATIONAL SEARCH REPORT

Information on patent family members

30/06/98

International application No.
PCT/FI 98/00257

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5535309 A	09/07/96	US 5355436 A	11/10/94
US 5467429 A	14/11/95	DE 69119172 D,T	09/01/97
		EP 0477486 A,B	01/04/92
		JP 2542107 B	09/10/96
		JP 4067257 A	03/03/92
		KR 9501601 B	27/02/95
		US 5166539 A	24/11/92
		US 5353383 A	04/10/94
		JP 4067258 A	03/03/92
		JP 4077865 A	11/03/92
		JP 4112362 A	14/04/92
		JP 4112354 A	14/04/92
		JP 4116719 A	17/04/92
		JP 4157566 A	29/05/92
		JP 4295976 A	20/10/92
		JP 4323723 A	12/11/92
US 5299285 A	29/03/94	NONE	